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(54) SINGLE-CHIP MICROCOMPUTER

(57) Abstract:

PURPOSE: To perform a high-speed interrupt multiplexing process without making software process by causing a priority register and level designating register to make multi-interrupt processes which are performed through mask register operations by means of software.

CONSTITUTION: A priority register 103 which designates a multi-interrupt processing level at every interrupt request and a level designating register 104 which designates an interrupt multiplexing level are provided and multi- interrupt is processed by these registers 101W104. In addition, a means which holds information indicating that a multi-interrupt level in the course of a multi- interrupt process is changed is set in the program status word 202 in a CPU 200. Therefore, even when the interrupt multiplexing level becomes deeper, updating information of multiple levels is held in a prescribed memory and the multiplexing level of the multi-interrupt becomes limitless. Therefore, a high-speed interrupt multiplexing process becomes possible without performing any software process.